Hysteresis Effect in Two-Dimensional Bi₂Te₃ Nanoplate Field-Effect Transistors

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1. Abstract

Recently field-effect transistors (FETs) based on two-dimensional (2D) Bi₂Te₃ nanoplates have attracted much attention due to their great potential for fabricating high-performance electronic devices. However, the gating property measurement of the Bi₂Te₃ nanoplate FETs exhibits hysteretic behaviour in an ambient environment, which degrades not only their electrical properties, but also their device performance. This work presents a systematical study on the origins of this hysteresis effect in 2D Bi₂Te₃ FETs and explores effective approaches to minimize and eliminate this hysteresis effect.

The hysteresis effect in 2D Bi₂Te₃ nanoplate FETs can be attributed to the charge trap states caused by the water molecules adsorbed on the nanoplate surface. To minimize and eliminate this hysteresis, poly (methyl methacrylate) (PMMA) layer is applied to passivate the 2D Bi₂Te₃ FETs, which leads to almost hysteresis-free gating property and thus improves the carrier mobility and device performance. These results indicate that the surface/interface trap states of nanostructures can significantly influence their electrical properties and thus device performance, and as a result surface passivation is required to minimize the influence of the surface/interface trap states and achieve high device performance.

2. Introduction

Semiconductor field-effect transistors (FETs) are the fundamental building blocks of the modern electronics industry and thus play a prominent role in people's daily life. With the development of electronic industry, FET devices are required to have better and better performance to meet the increasing performance demand. Over the past few years, two-dimensional (2D) materials, such as graphene, topological insulators (TIs), and transition metal dichalcogenides (TMDs), have attracted significant attention for fabricating high-performance FETs due to their unique physical properties such as high carrier mobility.^[1, 2] For example, Zomer et al. presented that the carrier mobility of graphene is as high as 12500 cm²V⁻¹s⁻¹, which makes it a promising material for potential applications in electronic devices. However, the graphene-based FETs exhibit

a few tens of $I_{\text{on}}/I_{\text{off}}$ ratio at most and large off-current, which is due to its zero bandgap.^[3] In comparison to graphene, the most significant advantage of TMDs is the existence of bandgap ranging from ~ 1 eV to 2 eV, ensuring a low off-current in switching behaviour and a small subthreshold swing of ~ 80 mV/dec.^[4] However, the relatively larger bandgap of TMDs is at the cost of carrier mobility. For example, the carrier mobility of MoS_2 presents only a few tens of $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ in experiments.^[5] In addition to TMDs and graphene, 2D Bi_2Se_3 -based transistors (one of TIs) were also investigated, which presented a narrow bandgap of 0.25 eV and a large $I_{\text{on}}/I_{\text{off}}$ ratio ($\sim 10^5$). This indicated its great potential in high-performance electronics, for example, infrared sensors.^[6]

Most recently, another TI material, Bi_2Te_3 , has received significant attention due to the interest in its fundamental physics (metallic surface states and strong spin-orbit interaction) as well as potential applications in FETs and infrared detectors.^[7, 8, 9] For example, Liu et al.^[10] reported FETs based on Bi_2Te_3 flakes with atomic-layer-deposited (ALD) Al_2O_3 as the top-gate and back-gate dielectric. They achieved both top-gate and bottom-gate control of the FETs, which presented different electron mobilities with ~ 1.69 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for the top-gate control and ~ 17.0 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for the bottom gate one. These results indicate that top-gate modulation is not as effective as the back-gate modulation, which is because the interface conditions and surface chemistry can significantly affect the field-effect modulation efficiency. Teweldebrhan et al.^[11] demonstrated FETs based on exfoliated Bi_2Te_3 films with Si/SiO₂ substrate as gate dielectric, which, however, did not show gate modulation with sweeping the gate

voltage from -50 V to 50 V at room temperature. Thus, this indicates extremely low carrier mobility. Chen et al. ^[12] studied the thermoelectric applications of Bi₂Te₃ nanoplates grown by chemical vapour deposition (CVD) method. They found that the grown Bi₂Te₃ nanoplates presented low thermopowers due to the unintentional surface doping (e.g. surface oxidation, gas adsorption, etc.), which can be improved by depositing 30 nm Al₂O₃ as a passivation layer. From these studies, it can be observed that the interface and surface conditions can have a significant influence on the carrier mobility and thus the device performance of 2D Bi₂Te₃ nanoplate-based FETs, which could limit their ultimate industry applications. The main reason can be attributed to the feature with 2D geometry, presenting almost all atoms exposed to the top/bottom surface. Apart from the interface and surface conditions such as different gate interfaces, the working environment can also have a significant influence on the device performance, which is currently missing for the study of Bi₂Te₃ nanoplate-based FETs. In this work, the influence of environmental conditions on the device performance is studied for Bi₂Te₃ nanoplate FETs. A hysteresis effect is observed for the Bi₂Te₃ nanoplate FET devices measured in an ambient environment when sweeping gate voltage forward and backward. Furthermore, the effect of various environmental conditions on the hysteresis effect is investigated systematically, including oxygen content, nitrogen molecules, and humidity to identify the main causes of this hysteresis effect. The physical mechanisms for this hysteresis effect are analyzed, and surface passivation is also studied to minimize this hysteresis effect and enhance the device performance.

3. Experimental Methods

Ultra-thin Bi_2Te_3 nanoplates with a thickness of ~ 10 nm in this work were grown in a 24-inch horizontal tube furnace (Lindberg/Blue M) by using CVD (chemical vapour deposition) method. The schematic growth system is presented in Figure S1. Bi_2Te_3 (Sigma-Aldrich, purity $> 99.99\%$) in powder form was used as precursor material, which was placed in a quartz boat located in the center of the furnace. Silicon substrates with 300 nm SiO_2 layer were used as the growth substrates and placed in another quartz boat located at downstream, which is 13-15 cm away from the central of the furnace. The detailed growth conditions were listed in Table S1 of the supporting information, and the detailed growth process has already been discussed in our previous studies.^[8, 9] The characterization results of the grown Bi_2Te_3 nanoplates, including Scanning Electron Microscope (SEM) images, Atomic Force Microscope (AFM) data, Raman spectrum, Energy Dispersive X-ray Spectrometer (EDS) data, and Transmission Electron Microscopy (TEM) results, have also been presented in our previous research.^[2, 8]

4. Results and Discussion

The schematic structure and SEM image of the Bi_2Te_3 nanoplate FET device are shown in **Figure 1a, b**, respectively. The metal electrodes of the 2D Bi_2Te_3 transistors were first defined by standard photolithography process on silicon substrate with a 300 nm SiO_2 layer on the top, then Cr (10 nm)/Au (40 nm) was deposited as metal contacts by using a conventional thermal evaporation process. The 300 nm SiO_2 layer that presents

a high-k dielectric was used to separate the gate electrode from the FET conducting channel. The electrical properties of Bi₂Te₃ nanoplate transistors in this work were measured in a probe station (Lakeshore TTP4) with a hermetic chamber at room temperature. Figure 1c presents the I_{ds} (drain current)-V_b (drain bias voltage) curves of the 2D Bi₂Te₃ transistor under a fixed V_g (gate bias voltage) of -30 V, 0V, and 30 V, respectively. The perfect linearity of the I_{ds}-V_b curves at the fixed V_g shown in Figure 1c indicates the ohmic nature of the Au contact. Figure 1d shows the gating features (I_{ds}-V_g) of the Bi₂Te₃ nanoplate FET with sweeping V_g from -30 V to 30V and then back to -30 V at a fixed V_b of 0.1 V. It is observed that the change of sweeping direction from forward to backward causes a significant threshold voltage (V_T) shift - up to ~ 12.5 V and reduces the I_{ds}, which leads to a big difference in the field-effect carrier mobility. Note that the hysteresis behaviour in this work is defined as the change of the V_T shift. According to the gating property, the field-effect mobility can be calculated by using the following equation:

$$\mu = \left[\frac{L}{CW} \right] \times \left[\left(\frac{dI_{ds}}{dV_g} \right) \right] \times \frac{1}{V_b}$$

, where C is the area-normalized capacitance of 300 nm thick SiO₂, C = 11.505 × 10⁻⁹ F/cm² for the 300 nm layer of SiO₂ (C = ε₀ε_r/d; ε₀ = 8.85 × 10⁻¹² F/m; ε_r = 3.9; d = 300 nm), W is the channel width of the Bi₂Te₃ transistor, L is the channel length of the device, I_{ds}, V_b and V_g have been defined above. In this work, L and W are approximately 10 μm and 11 μm, respectively. Based on this equation, the Bi₂Te₃ nanoplate FET device shows an electron mobility of 10.9 cm²V⁻¹ s⁻¹ and 21.4 cm²V⁻¹ s⁻¹

¹ for the forward and backward sweeping V_g , respectively. Note that although it is for the first time observed in 2D Bi_2Te_3 nanoplates, this hysteresis phenomenon and the degradation of the device performance were also observed in other nanostructured materials, such as graphene and MoS_2 ,^[13, 14] which were mainly attributed to water and oxygen molecules-related trapping states. In the meantime, the relatively lower mobility of the Bi_2Te_3 nanoplate FETs observed in this work also suggests the presence of trapping states.

Considering the fact the hysteresis effect is observed at a fixed V_b while sweeping the V_g , the carrier transport and device behaviour could be affected by the trapping states in the Bi_2Te_3 nanoplates and/or those at the interfaces between the Bi_2Te_3 nanoplates and air/ SiO_2 . Therefore, there are three possible types of trapping states existed in the devices of this work, which is sketched in Figure 1a: (1) the adsorbates on the Bi_2Te_3 nanoplate surface. For example, water molecules adsorbed on the nanoplate surface; (2) the intrinsic defects in the Bi_2Te_3 nanoplate; and (3) extrinsic traps at the interface between Bi_2Te_3 nanoplate and SiO_2 . Because the Bi_2Te_3 nanoplates were grown under vacuum environment and at a high temperature of over 400°C , and special attention has been devoted to removing the possible residues of air before starting the growth, it is unlikely for water/oxygen molecules to appear at the $\text{Bi}_2\text{Te}_3/\text{SiO}_2$ interface, eliminating the origin of type (3) trapping states. Although oxygen vacancies in materials can cause hysteresis effect as observed in ZnO nanowire FETs,^[13, 15] it is unlikely for Bi_2Te_3 nanoplates to have oxygen vacancy, thus ruling out the origin of type (2) trapping states. As shown by the high resolution TEM study of the Bi_2Te_3 nanoplate, no oxygen

vacancy were observed.^[2, 9] As a result, type (1) trapping states are the main reason for the hysteresis effect observed, which will be studied in details in the following.

Figure 1. a) Sketch of the fabricated Bi₂Te₃ nanoplate-based FETs; b) SEM image of a FET based on Bi₂Te₃ nanoplates shown in (a); c) I_{ds} - V_b curves acquired with a V_g values of -30, 0 and 30 V; d) Hysteretic behaviour of I_{ds} - V_g measured at a fixed gate bias voltage V_g . Arrows in (d) indicate the sweeping directions of V_g .

Figure 2a shows the transfer curves of the Bi₂Te₃ nanoplate FET device measured in the air before and after baking at 120 °C for 2 hours in a vacuum tube with flushing argon gas. It is observed that the V_T shift caused by hysteresis is decreased to 1.5 V

after baking, indicating that the adsorbates on the device surface such as water, oxygen and nitrogen from the air, could be the primary causes for the hysteresis observed here. The small shift of V_T observed after the furnace baking in Figure 2a could be related to the re-adsorbed molecules on the device surface from the air during the cooling process after baking. To study the specific origin for the hysteresis observed, the 2D Bi_2Te_3 nanoplate-based FETs were measured under different measurement conditions in the probe station chamber at a fixed V_b of 0.1 V. First, to study the influence of oxygen molecules in the air the I_{ds} - V_g features of the 2D Bi_2Te_3 FET were measured in the testing chamber filled with pure dry nitrogen and dry air, respectively, as shown in Figure 2b. It can be seen from Figure 2b that there is no significant difference in the hysteresis observed, which indicates that the influence of oxygen can be excluded as the main cause of the hysteresis effect. Another possible adsorbate on the nanoplate surface is nitrogen molecules in the air, which also could be the reason for the hysteresis. Figure 2c presents the gating property of 2D Bi_2Te_3 FETs measured under vacuum (10^{-4} Torr) and under dry nitrogen filled testing environment with a nitrogen pressure of 772 Torr, respectively. The change in the V_T is 1.5 V under vacuum, and 1.35 V under the nitrogen pressure of 772 Torr, respectively, which are much smaller in comparison to the results as shown in Figure 1d. This proves that the nitrogen molecules in the air are also not the main reason for the hysteresis effect observed. As a result, water molecules adsorbed on the device surface could be the main possible origin for the hysteresis effect.

To study the influence of water molecule adsorption, the 2D Bi₂Te₃ nanoplate-based FET was measured in an environment with various concentrations of water molecules (C_{wm}), which ranged from dry air (C_{wm} : 2%) to a higher C_{wm} of 40 %. As shown in Figure 2d, the V_T shift caused by the hysteresis increases from 1.5 V to 12.5 V with increasing the C_{wm} in the test chamber from 2% to 40%. Table S2 of the supporting information shows the summary of the V_T shift with adjusting C_{wm} (device 1). To confirm the durability of the hysteresis effect, other two devices were measured under the same conditions, presenting similar value of V_T shift. These results clearly indicate that the C_{wm} in the air is the main cause for the hysteresis effect observed in this work. The reason of this C_{wm} -induced hysteresis can be attributed to the fact that water molecules can act as acceptor-type traps with negative charges, and thus cause the Fermi energy level of the Bi₂Te₃ channel to be filled with electrons. This will lead to different Schottky barrier heights and current decay rates, and thus the hysteresis effect observed above ^[16]. It should be noted that for nanostructured devices the effect of charge traps and thus hysteresis effect could be more significant in comparison to that in devices with large sizes, which degrades the device performance more seriously.^[17] As a result, for nanostructured devices such as Bi₂Te₃ nanoplate FET in this work, it is essential to further study the trapping behaviour to understand the hysteresis mechanism and identify approaches to minimize the hysteresis effect in order to achieve high device performance, which will be discussed next in more details.

Figure 2. a) Hysteresis behaviour of the Bi_2Te_3 nanoplate-based transistor measured with and without baking process; b) Hysteretic behaviour of $I_{\text{ds}}\text{-}V_{\text{g}}$ for the same device measured in the chamber filled with dry air and dry N_2 , respectively; c) Hysteretic behaviour of $I_{\text{ds}}\text{-}V_{\text{g}}$ for the same device measured under vacuum and dry N_2 ; d) Hysteresis evolution of the same transistor under different humidity.

In order to further understand the hysteresis effect caused by charge traps, the transient characteristics of I_{ds} were measured at a fixed V_{g} of 30 V and a V_{b} of 0.1 V, the results of which are shown in **Figure 3a-d**. One of the most important parameters for estimating the charge traps in a device is the trapping time constant, which determines not only the effective carrier density in a semiconductor material but also the noise behaviour of a FET. The data in Figure 3a-d are fitted by using the following equation:

$$I = I_0 + Ae^{\frac{-t}{t_1}}$$

, where t_1 is a trapping time constant. Figure 3a shows the results measured in an environment filled with dry air (C_{wm} : 2%). It is observed that I_{ds} decays exponentially with time, characterized by the decay time constant of t_1 to be 133.40 s. Figure 3b-c show the transient characteristics of the device measured in the chamber filled with different C_{wm} (20% and 40%) of air. It is observed that the device measured under the higher C_{wm} exhibits a faster decay of I_{ds} . Moreover, the time constant of t_1 for the cases measured with a C_{wm} of 20 % and 40% are fitted to be 54.14 and 25.80 s, respectively. The time constant (t_1) clearly follows a downward trend with increasing C_{wm} from 2% to 40%. This indicates that a higher C_{wm} can lead to a relatively faster current decay and thus a smaller time constant, which is mainly due to the higher concentration of trapping states existed on the device surface when have a higher C_{wm} .

In comparison to the trapping time constants reported in other works,^[18] the time constants obtained in this work are much larger, which indicates the hysteresis in 2D Bi_2Te_3 FETs is a relatively slow process. Therefore, it means that this hysteresis can be observed only when the sweeping rate of V_g is slow. Figure 3d shows the Bi_2Te_3 nanoplate FETs measured with two different sweeping rates of 0.75 V/s and 1.5 V/s, respectively. It is observed that the hysteresis effect weakens with a larger sweeping rate. This is mainly due to the fact that with a high sweeping rate and a larger decay time constant the device does not have enough time to collect carriers from those trapping states, leading to a weakened hysteresis effect observed.

Figure 3. Transient characteristics of drain-current (I_{ds}) at a fixed gate voltage of 30 V and a drain bias voltage of 0.1 V measured under a) dry air (C_{wm} : 2%), b) C_{wm} : 20% and c) C_{wm} : 40%. d) Hysteretic behaviour of I_{ds} - V_g at a fixed bias voltage of 0.1 V under different sweeping rates of V_g .

As discussed above, the trap states on the Bi_2Te_3 nanoplate surface are mainly caused by the adsorption of water molecules in the air, and present relatively a larger trapping time-constant. To quantify the water-induced trap states, the density of trap states (D_{ts}) for the Bi_2Te_3 nanoplate FETs under different C_{wm} are extracted and analyzed by using

a subthreshold method reported before ^[19]. First, the I_{ds} near the subthreshold regime can be expressed using the following equation:

$$I_{ds} = I_M \left[1 - e^{-\frac{qmV_b}{nkT}} \right]$$

Where $n = 1 + \frac{C_d + C_{it}}{C_{ox}}$, $m = 1 + \frac{C_d}{C_{ox}}$, C_d is the depletion capacitance per unit, C_{it} is the interface capacitance per unit area, C_{ox} is the area-normalized capacitance of 300 nm thick SiO_2 , V_b is the bias voltage and I_M is the maximum drain current at the given V_g , k is the Boltzmann's constant, q is the elementary charge, and T is the temperature.

Then $\frac{m}{n} \times V_d = \frac{-\ln\left(1 - \frac{I_{ds}}{I_M}\right) \times k \times T}{q}$. Thus the values of $\frac{m}{n}$ for the device measured under different C_{wm} can be obtained *via* the ratio of the $\frac{-\ln\left(1 - \frac{I_{ds}}{I_M}\right) \times k \times T}{q}$ to the V_d . The

value of n can be extracted from the subthreshold slope of the transfer characteristics for our devices measured under different C_{wm} : $n = \frac{Sq}{2.3kT}$ where S is the subthreshold

slope, q , k and T are defined above. S can be extracted from the ratio of the V_g to $\log I_{ds}$. Thus, the values of n , $\frac{m}{n}$ and S under different C_{wm} and different V_g can be

calculated, the values of which are listed in Table 1. The D_{ts} of the Bi_2Te_3 nanoplate

FETs can then be calculated using the equation: $D_{ts} = \frac{C_{it}}{q} = \frac{C_{ox}}{q} \times (n - m)$. **Figure**

4a shows the dependence of D_{ts} on the V_g under different C_{wm} at a V_d of 0.1 V. It is observed that the value of D_{ts} can be up to $6.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ under the C_{wm} of 40% at a V_g of 30 V, however, the D_{ts} can be reduced to $1.2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ under the C_{wm} of 2% at a V_g of -30 V. This further confirms that a higher C_{wm} in the testing chamber can induce a higher D_{ts} which act as carrier trapping centres and leads to the hysteresis effect and device performance degradation observed. Also, the increased D_{ts}

with increasing V_g under different C_{wm} indicates that the water-induced trap states are mainly located at shallow energy levels, which are close to the conduction band and are shallow traps.^[20]

Figure 4. Dependence of the trap density on V_g for C_{wm} varying from 2% to 40%.

Table 1. summary of the extracted and calculated parameters under different V_g and C_{wm} , including D_{ts} , n , m and S .

	V_g (V)	D_{ts} [$cm^{-2} eV^{-1}$]	n	m	S [mV/dec]
C_{wm} : 40%	-30	1.35×10^{11}	2.78	0.903	0.162
	-20	1.74×10^{11}	2.74	0.320	0.159
	-10	1.92×10^{11}	2.75	0.080	0.160
C_{wm} : 20%	-30	1.02×10^{11}	2.65	1.231	0.154
	-20	1.23×10^{11}	2.58	0.869	0.150
	-10	1.46×10^{11}	2.64	0.610	0.153
C_{wm} : 2%	-30	8.7×10^{10}	2.55	1.340	0.148
	-20	9.8×10^{10}	2.46	1.097	0.143
	-10	1.18×10^{11}	2.52	0.879	0.146

To better understand the physical mechanism, it is essential to study the energy band diagram of the Bi_2Te_3 nanoplate FET which is plotted in **Figure 5a**. As illustrated in Figure 5a, the adsorbed water molecules tend to form acceptor-type traps with negative charges and thus result in trap energy levels filled with electrons. Therefore, when water molecules are adsorbed on the Bi_2Te_3 nanoplate surface, the electrons can be transferred to the water molecules, which behave as a “doping” process. Because of this doping process, the Fermi level (E_F) is moved down toward the valence band (E_V).^[21] The Schottky barrier height which is defined as the difference of the E_F between the metal contact and the Bi_2Te_3 channel also increases when having water molecules on the Bi_2Te_3 nanoplate surface. A higher Schottky barrier height will result in a larger contact resistance and wider tunnelling width, leading to the degradation of device performance.

It should also be noted that when measuring the I_{ds} - V_g curves under different C_{wm} , the V_T measured with sweeping the V_g forward from -30 V to 30 V is much less than that with sweeping the V_g backward from 30 V to -30 V, as presented in Figure 2d. This observation can also be explained by the water-induced acceptor-type trap states on the surface of Bi_2Te_3 channels. As illustrated in Figure 5b, the water-induced acceptor-type states are filled with negative charges, which leads to the Fermi energy level filled with electrons and thus lift the Fermi energy level. On one hand, the electrons captured by the water-induced trap states can be released to the Bi_2Te_3 channel with scanning V_g forward from -30 V to 30 V, which is due to the negative V_g applied initially and thus the reduced V_T caused. On the other hand, electrons are transferred to the water-induced traps with sweeping the V_g backward from 30 V to -30 V due to the positive V_g applied

initially, and thus the increased V_T caused.^[21] As discussed above, water molecules adsorbed on the Bi_2Te_3 channel are the main reason for the hysteresis behaviour observed in this work.

Figure 5. a) Schematic diagram of the energy band along the Bi_2Te_3 channel and the metal contacts before and after the removal of water molecules in the air. b) energy band diagram of the Bi_2Te_3 channel with adsorbed water molecules as trap states filled with electrons below the Fermi level (E_F).

As the hysteresis behaviour will degrade the electrical properties and thus the ultimate device application, it is necessary and vital to explore effective methods to minimize and even eliminate this hysteresis behaviour in the 2D Bi_2Te_3 FETs. It is known that surface passivation can effectively suppress and eliminate the influence of surface states and thus enhance the performance of electronic devices such as transistors and infrared detectors.^[22] To overcome this hysteresis effect, photoresist PMMA is used as a

passivation layer to suppress and eliminate the hysteresis effect observed in the Bi_2Te_3 FETs. **Figure 6a** shows the schematic diagram of 2D Bi_2Te_3 nanoplate FET passivated with PMMA thin layer. The detailed fabrication process is as follows: first, PMMA was naturally warmed-up to room temperature, and coated onto the 2D Bi_2Te_3 FET for 60 s at a rotational speed of 3000 r/min by using a spinner; then, the pattern of the two electrodes was defined on the coated PMMA layer with a standard photolithography process; at last, the device was baked at 120°C for 120 s to solidify the PMMA. Note that the passivation process was conducted under atmospheric pressure in a class 1000 cleanroom and the devices were baked at 120 °C for 2 hours before coating the PMMA passivation layer. Figure 6b shows the hysteresis behaviour of the 2D Bi_2Te_3 FETs measured with PMMA passivation layer under different scanning rates of V_g . It can be observed that the devices passivated with PMMA layer present almost hysteresis-free I_{ds} - V_g curve and thus a significantly enhanced carrier mobility ($\sim 43.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), even under the low scanning rates of 0.75 V/s. This much-improved device performance can be attributed to the outstanding hydrophobic property of PMMA which could prevent Bi_2Te_3 nanoplate surface from adsorbing water molecules in the air.

It should be noted that a weak hysteresis effect ($\sim 0.15 \text{ V}$) is still observed in PMMA-passivated 2D Bi_2Te_3 FETs, as presented in Figure 6b, which can be attributed to the water molecules permeated through the PMMA layer from the air or the water molecules remained on the nanoplate surface even after the 2h's baking at 120 °C before passivation. Although the Bi_2Te_3 nanoplates grown in this work have a high crystalline quality, there could be some surface defects on the nanoplates. Because the water

molecules in the air prefer to be adsorbed on the crystal defects with higher binding energy, it is hard to remove these water molecules adsorbed due to the stronger bonds with the structure defects. Therefore, high quality Bi_2Te_3 nanoplates without intrinsic defects will also be critical for reducing and eliminating the hysteresis effect, and thus enhancing the device performance. In addition, as seen in Figure S2, to further confirm the durability of the passivated FETs after long-term storage in air, we also measured the hysteretic effect of the PMMA-passivated FETs under the same conditions before and after the long-term storage. There is no obvious difference observed before and after the storage, further indicating that the PMMA layer presents great potential to prevent Bi_2Te_3 nanoplate surface from adsorbing water molecules from the air and thus eliminate the hysteresis effect.

Figure 6. a) Schematic diagram of the Bi_2Te_3 nanoplate-based transistor passivated with a PMMA layer. b) hysteric behaviour in the same device with PMMA passivation under different scanning rate of V_g .

5. Conclusion

In this work, we have systemically investigated the hysteresis behaviour for the first time in 2D Bi₂Te₃ nanoplate FETs. It is observed that, when measuring the gating property, the threshold voltage in 2D Bi₂Te₃ nanoplate FETs is changed from -17.5 V to -5 V with sweeping the gate voltage from forward to backward. To study the origin of this hysteresis behaviour, the I_{ds} - V_g features and transient characteristic of 2D Bi₂Te₃ nanoplate FETs are measured under different nitrogen, oxygen, and humidity environments. The trap states caused by water molecule adsorption on the Bi₂Te₃ nanoplate surface are found to be the primary reason for this hysteresis behaviour. Fundamentally, this hysteresis effect observed might be attributed to the electrons of Bi₂Te₃ channel captured by the water-induced acceptor-type trap states. To minimize and eliminate this hysteresis effect, PMMA passivation is applied to prevent the water adsorption on the nanoplate surface, which leads to a significantly reduced hysteresis effect and an enhanced device performance. This work demonstrates that the interface/surface chemistry of 2D materials can significantly impact their electrical properties, and thus their ultimate device performance. The surface passivation can effectively reduce the surface states and thus enhance their device performance, which can also be applied to other 2D material-based electronic devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author

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Table of contents:

J. Liu[†], Dr. W. Pan[†], H. Wang, Z. Zhang, S. Zhang, G. Yuan^{*}, C. Yuan, Y. Ren, W. Lei^{*}

Title: Hysteresis effect in Two-dimensional Bi₂Te₃ Nanoplate Field-Effect Transistors

Hysteresis effect is observed for the first time in the Bi₂Te₃ nanoplate Field-Effect Transistors (FETs). The hysteresis effect degrades the carrier mobility and can be attributed to the water molecules-related trapping states. To minimize this hysteresis effect, poly (methyl methacrylate) layer is applied to passivate the 2D Bi₂Te₃ FETs, which leads to almost hysteresis-free FETs based on Bi₂Te₃ nanoplates.